

MS-7676 Ver: 3.1 m-ATX : 245 X 245mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(Z68)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UP1625 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: IP6103

CPU SA : OP+MOS

DDR: UP6103

PCH: UP6103

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

USB3.0 RearX2

D-SUB/DVI/HDMI *1

TPM Header *1(debug only)

on BOARD BUZZER

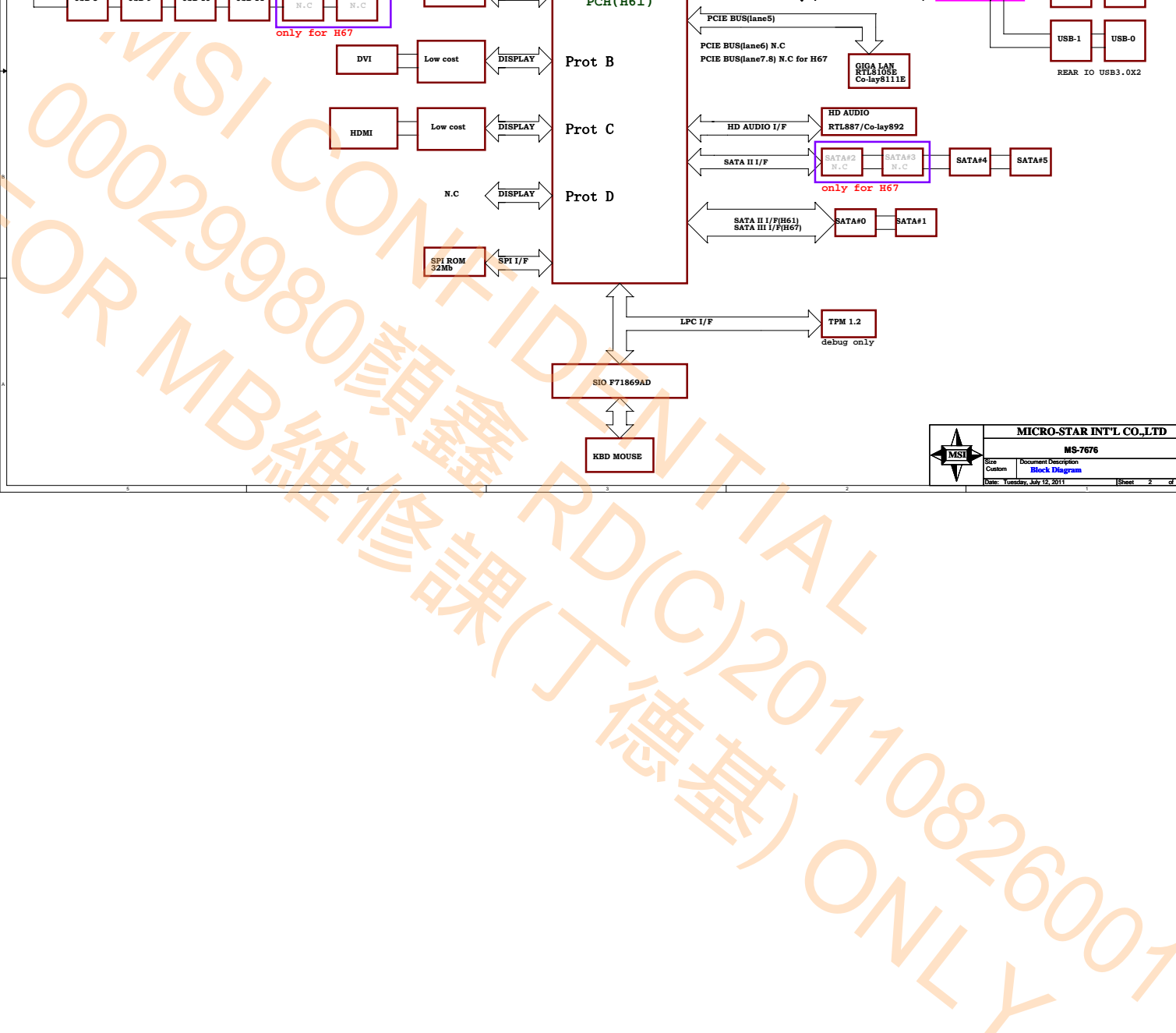
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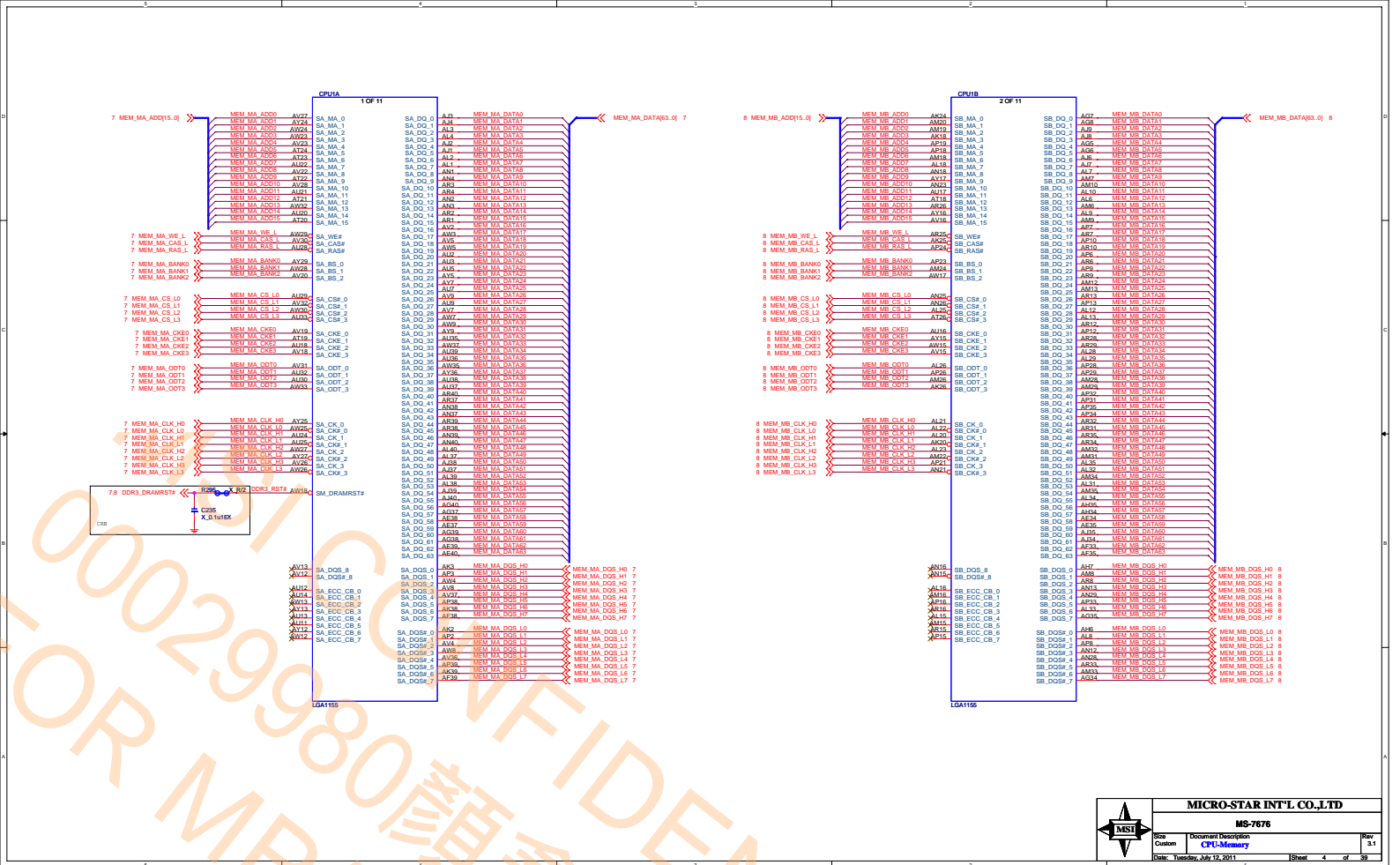
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BOM:

- 1.H67 Full Spec(mil)
- 2.H61 Full Spec(mil)
- 3.H61 common Spec(mil)

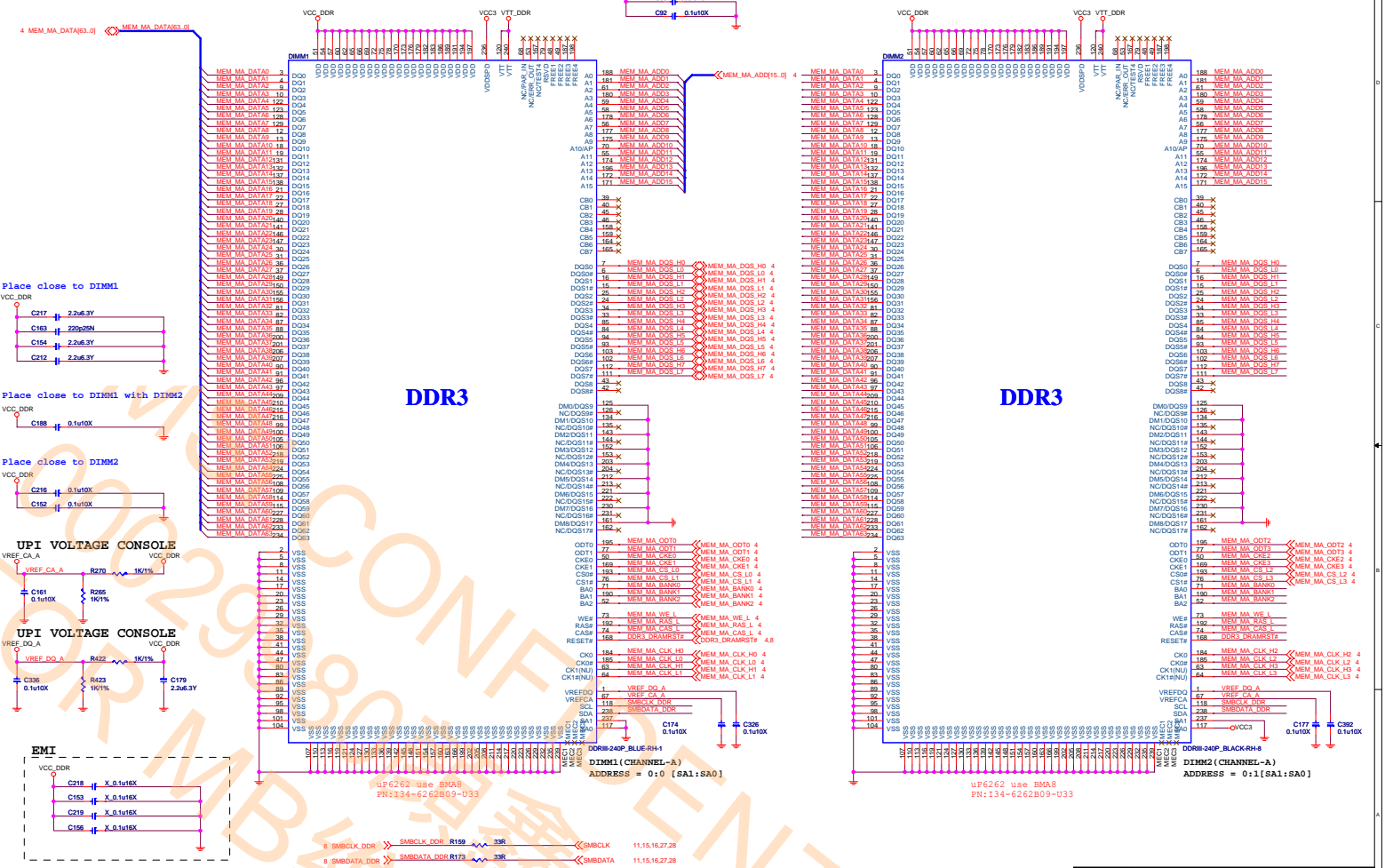
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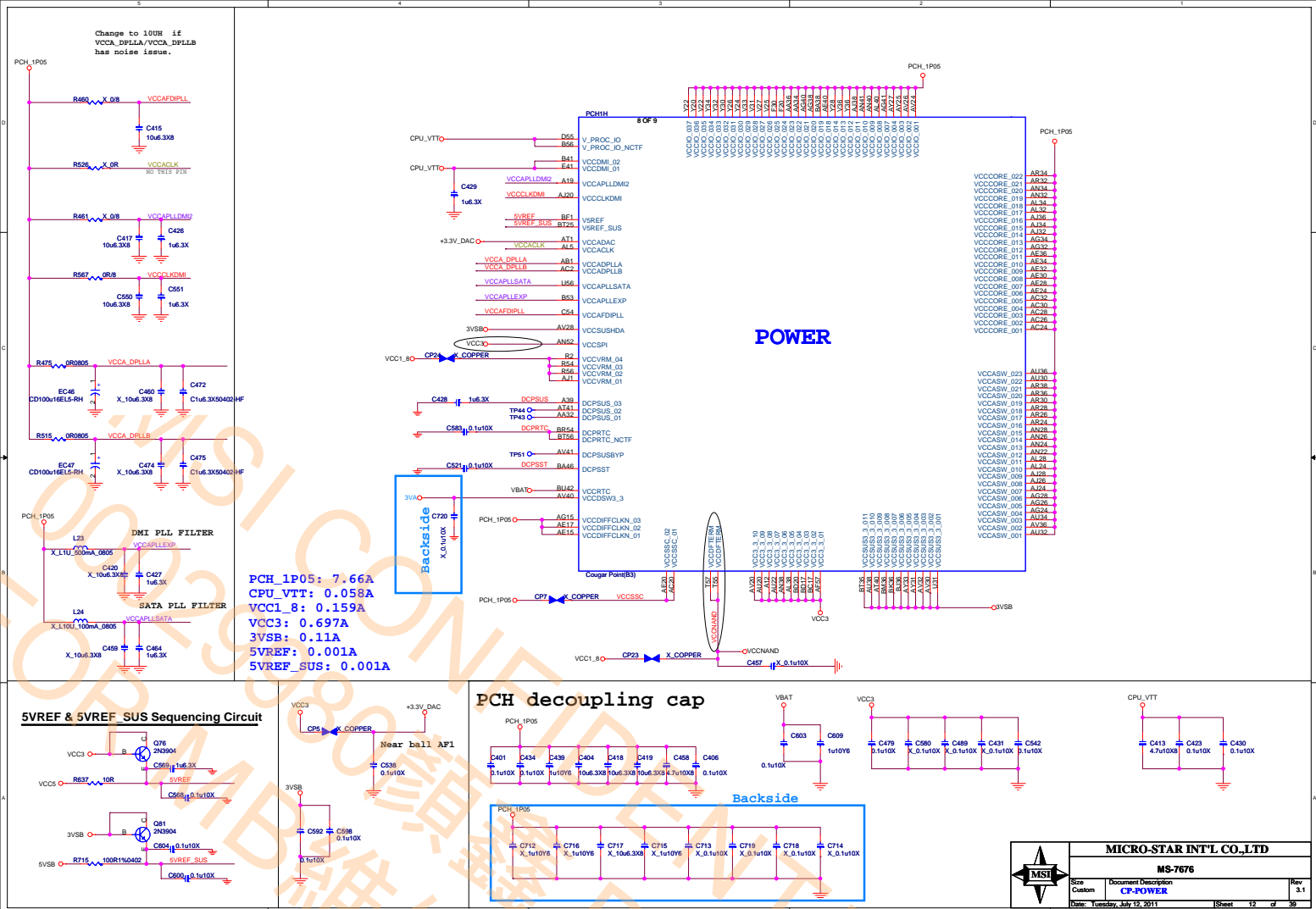
DDR3 DIMM_A0

DDR3 DIMM_A1



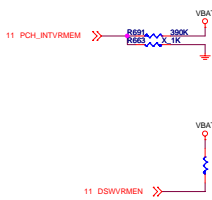
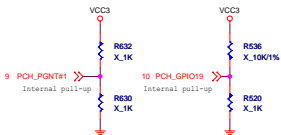
DDRIII DIMM_B1





PCH Straps

BOOT DEVICE	GNT1	SATA/GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

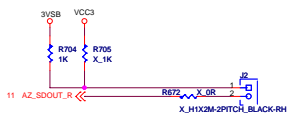
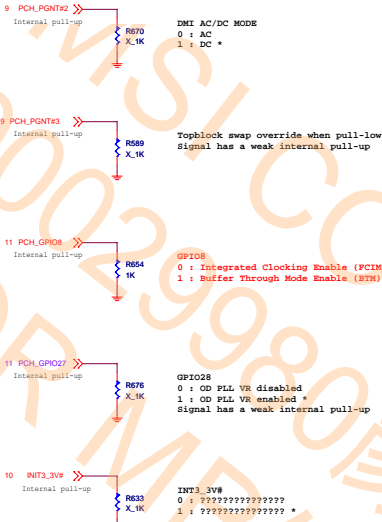


INTVRMEM
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GBW only operates at 10/100 Mbps during S3-S5.

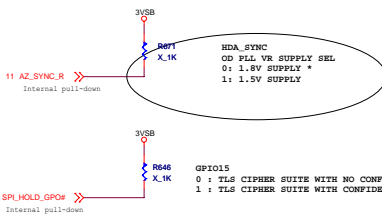
DSVMEM
0: Disable Internal Deep Sleep 1.05 V regulators.
1: Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.



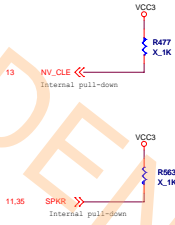
HDA_SDO
Disable MS in Manufacturing Mode when pull LOW ???

HDA_SDO has internal pull down. Default should be connected to SDIN of codec, no pull up/down. To Disable MS need to have a jumper to pull high



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.5V SUPPLY *
1: 1.5V SUPPLY

GPI015
0: TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1: TLS CIPHER SUITE WITH CONFIDENTIALITY



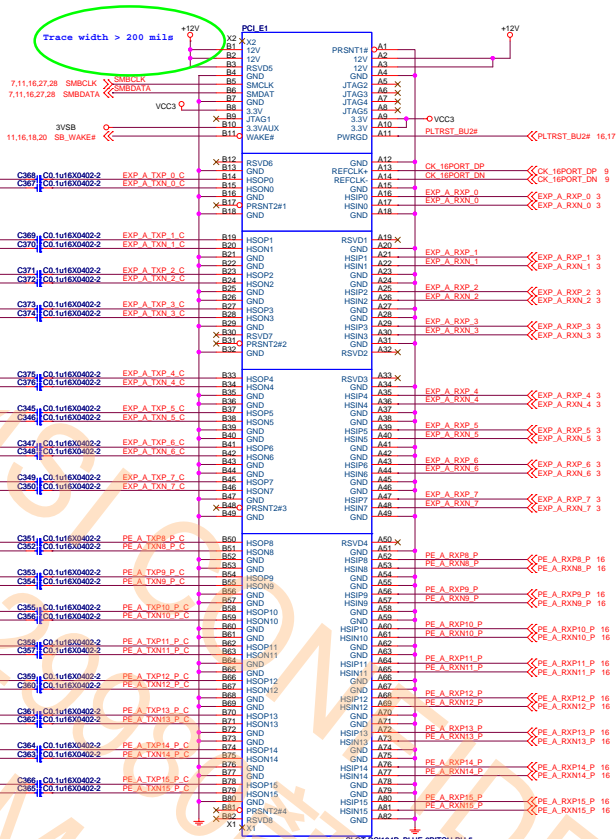
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC I2S SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW **
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

SPWR
0: EN TO REBOOT *
1: DIS TO REBOOT

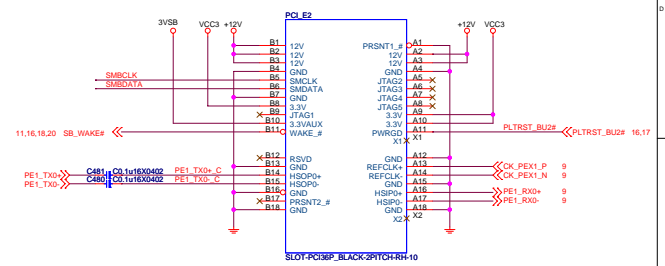
1: INIT3_3V# to asserted for 16 PCI clock to reset the processor by some events occur.
0: Can not to reset the processor.

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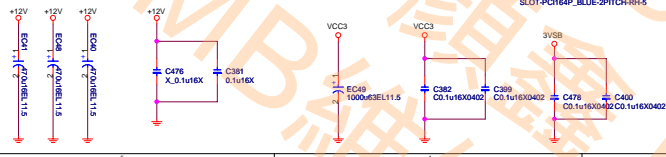
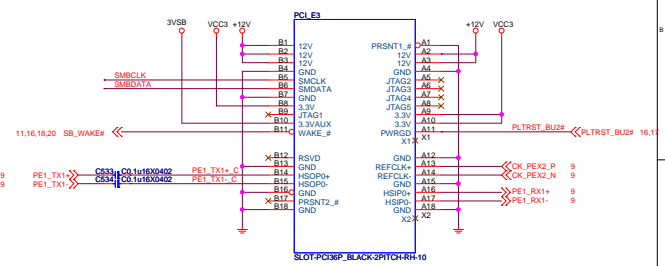
PCI Express X16 Slot



PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT

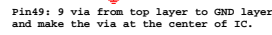


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Custom	PCIe x16 h1/x1	3.1
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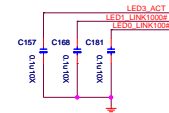
~~(Share with PCI_E x16 Slots)~~



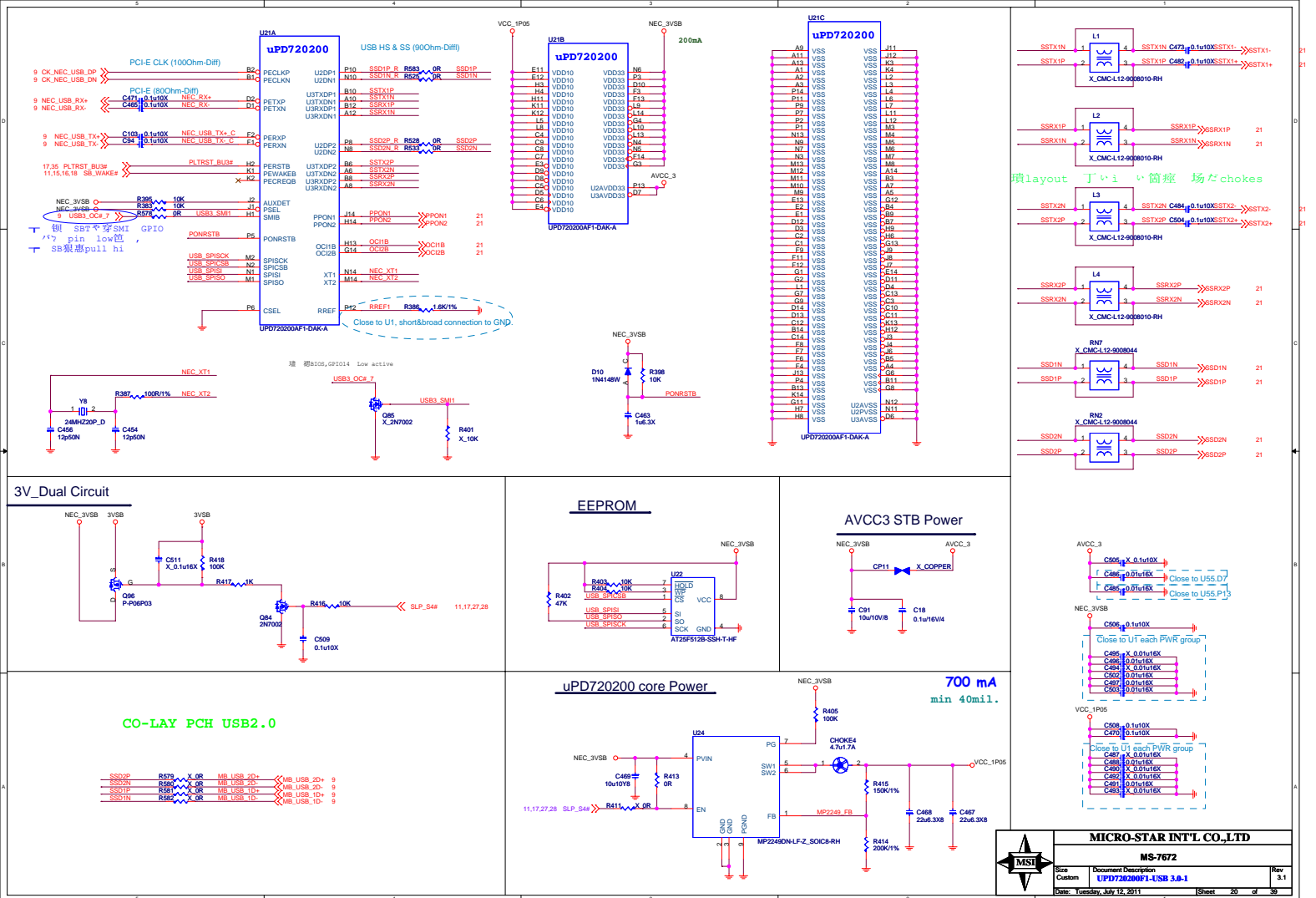
RTL8105E 10/100M LAN



10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



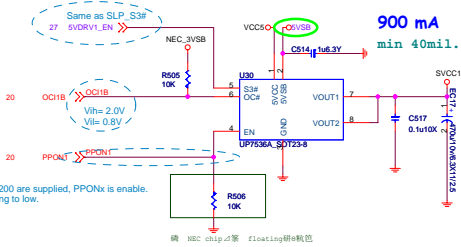
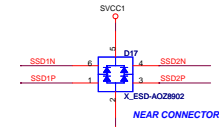
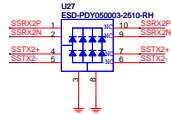
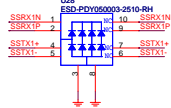
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Rear I/O

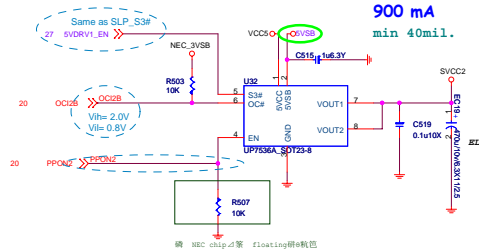
ESD Protection

Close to Connector



All power sources of uPD72020 are supplied, PPOnx is enable.
PPOnx is low when OC1x going to low.

請 NRC chip 旁 floating 腳 0 軌

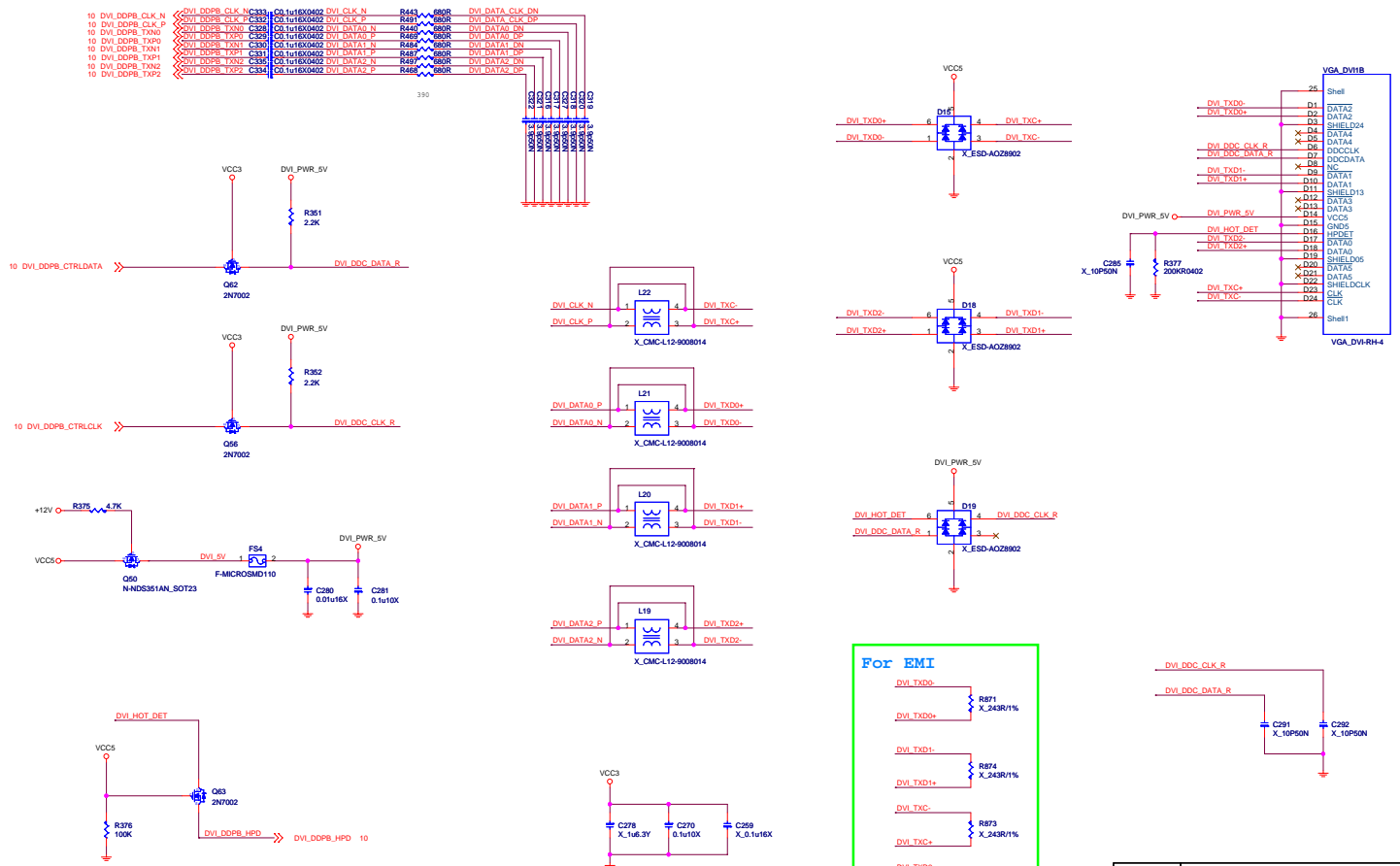


請 NRC chip 旁 floating 腳 0 軌

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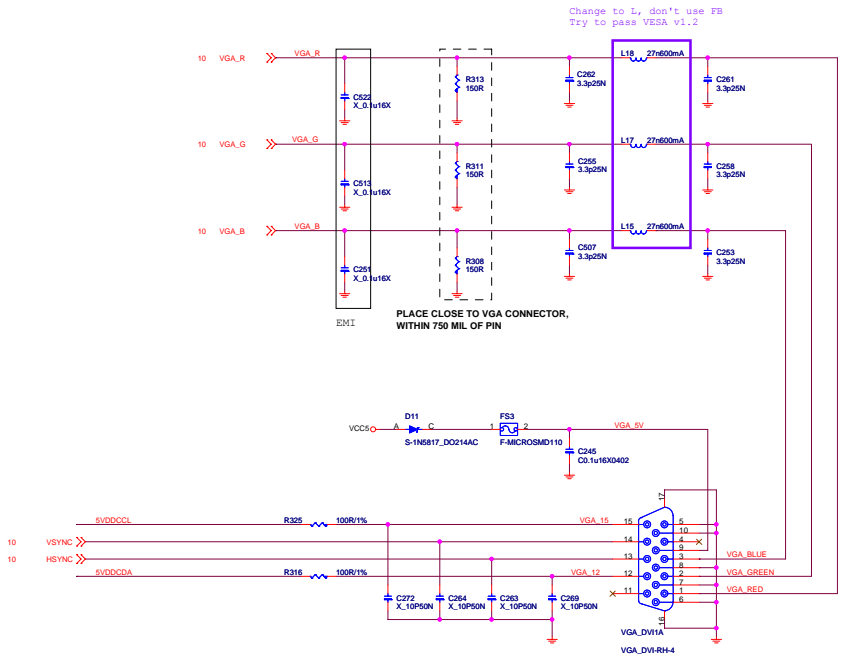
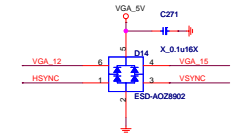
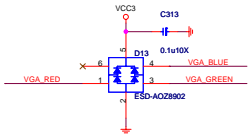
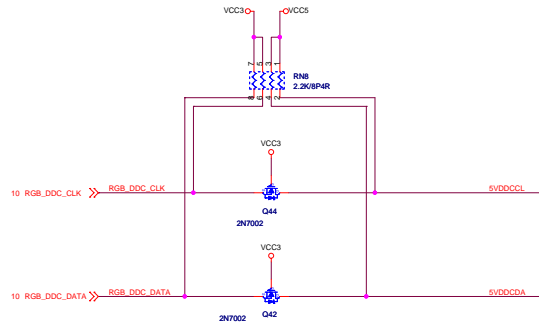
DVI level shifter


VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



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Custom	DVI transfer	3.1	
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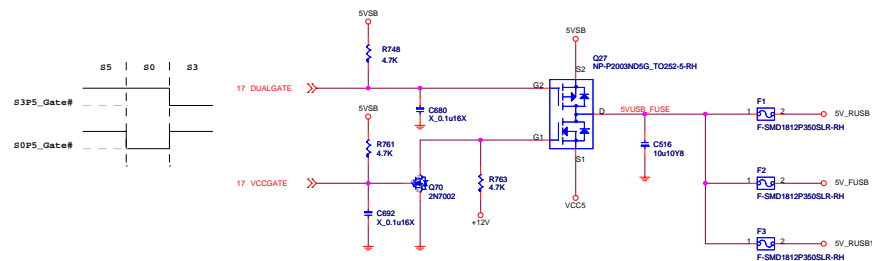
Level shift



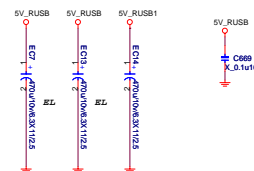


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Custom	VGA	3.1
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5V_USB Switch



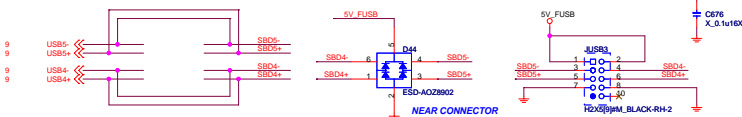
NEAR USB REAR CONNECTOR



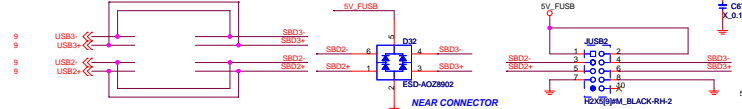
Front USB Connector

For H61 6,7,12,13 Port should be remove

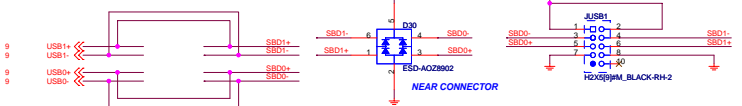
FRONT USB PORT 4,5



FRONT USB PORT 2,3

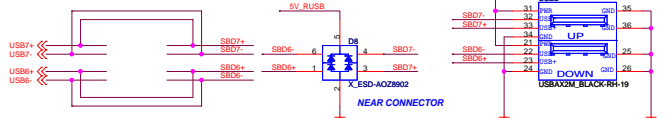


FRONT USB PORT 0,1

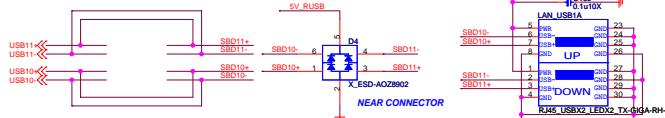


Rear USB Connector

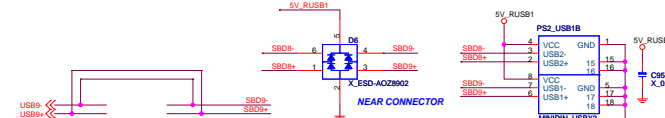
REAR USB PORT 6,7 (With HDMI)



REAR USB PORT 10,11 (With LAN)

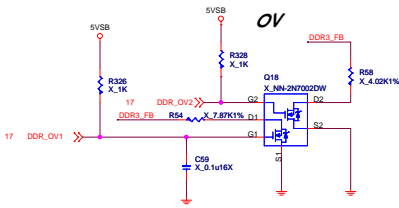


REAR USB PORT 8,9 (With PS2)



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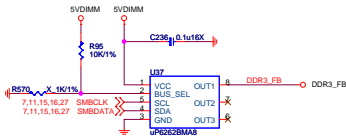
DDR3_1.5V 4.5A+7.5A+1A=13A
 4.5A FOR CPU
 7.5A FOR 2DIMM
 1A FOR DDR VTT



*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPT001(S/IO)
 DDR_OV2 = GPT002(S/IO)

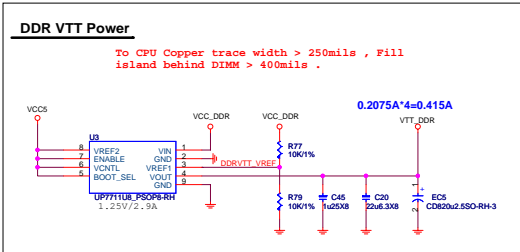
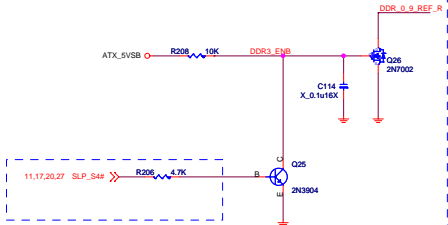


UPI VOLTAGE CONSOLE

0x20 : RH=10K, RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

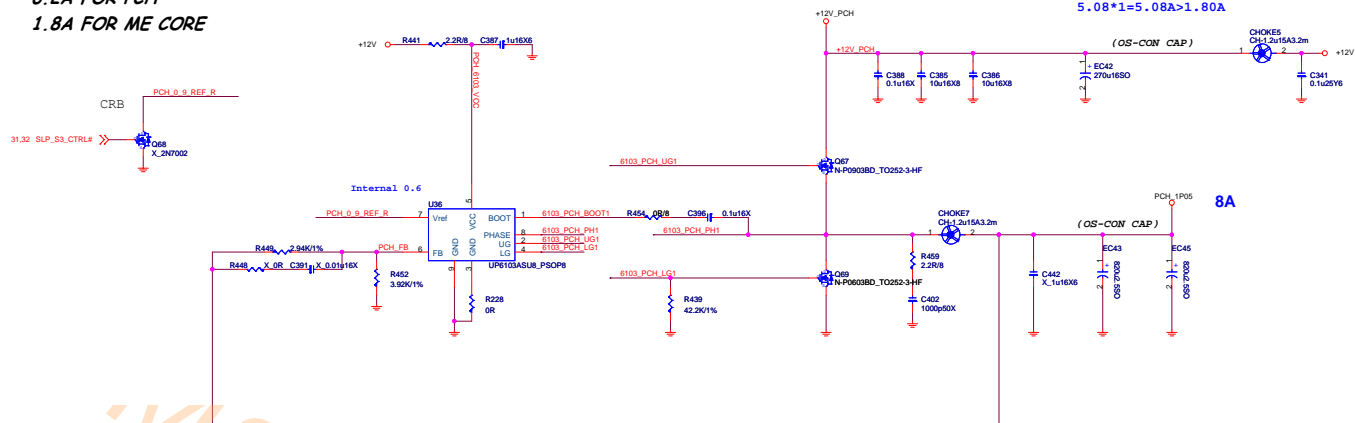
P.S. Only for meet Intel power down sequence.



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Custom	DDR Power - nP6103 1-Phase	3.1	
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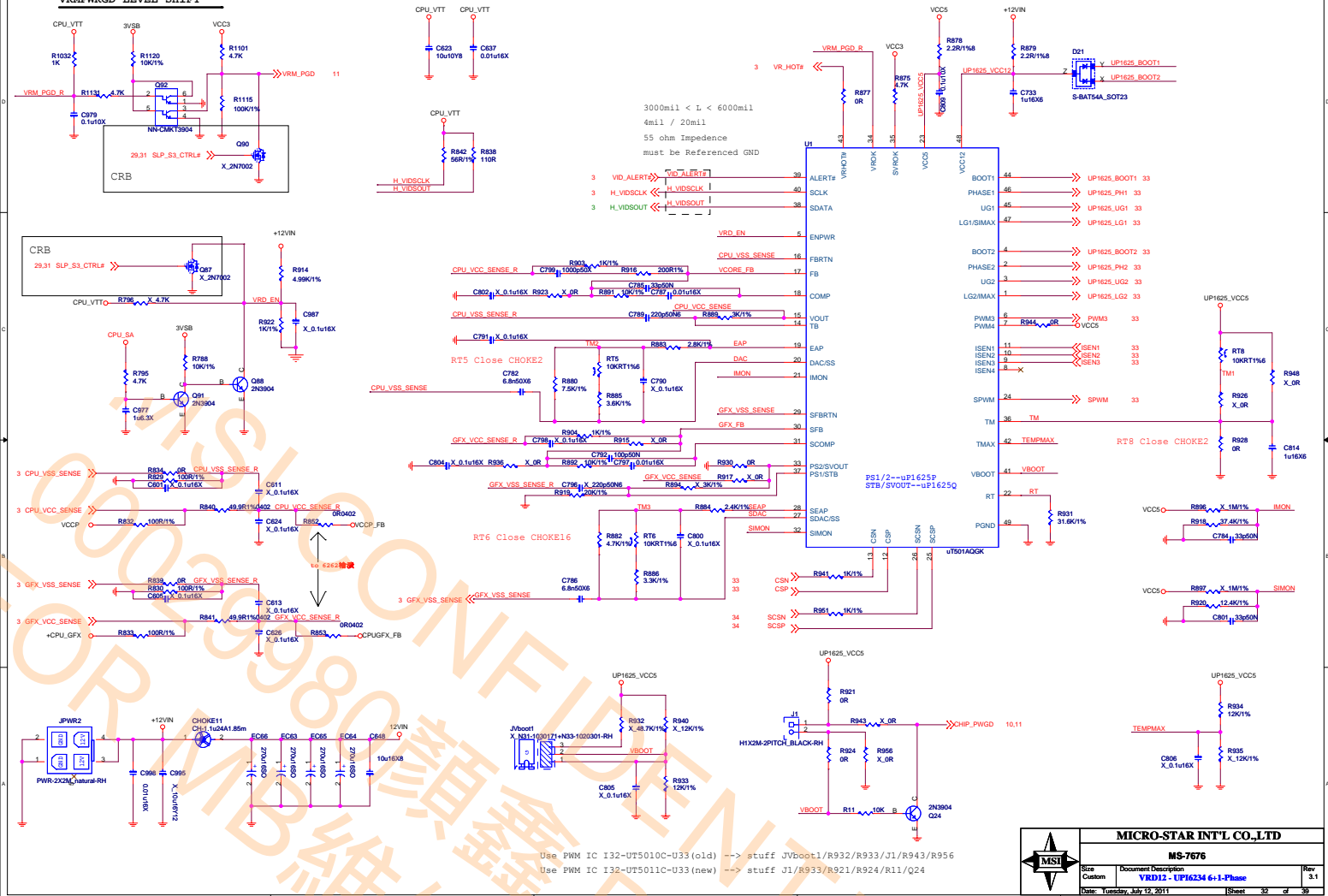
PCH Power:1.05V
PCH Core 6.2A+1.8A=8A
6.2A FOR PCH
1.8A FOR ME CORE

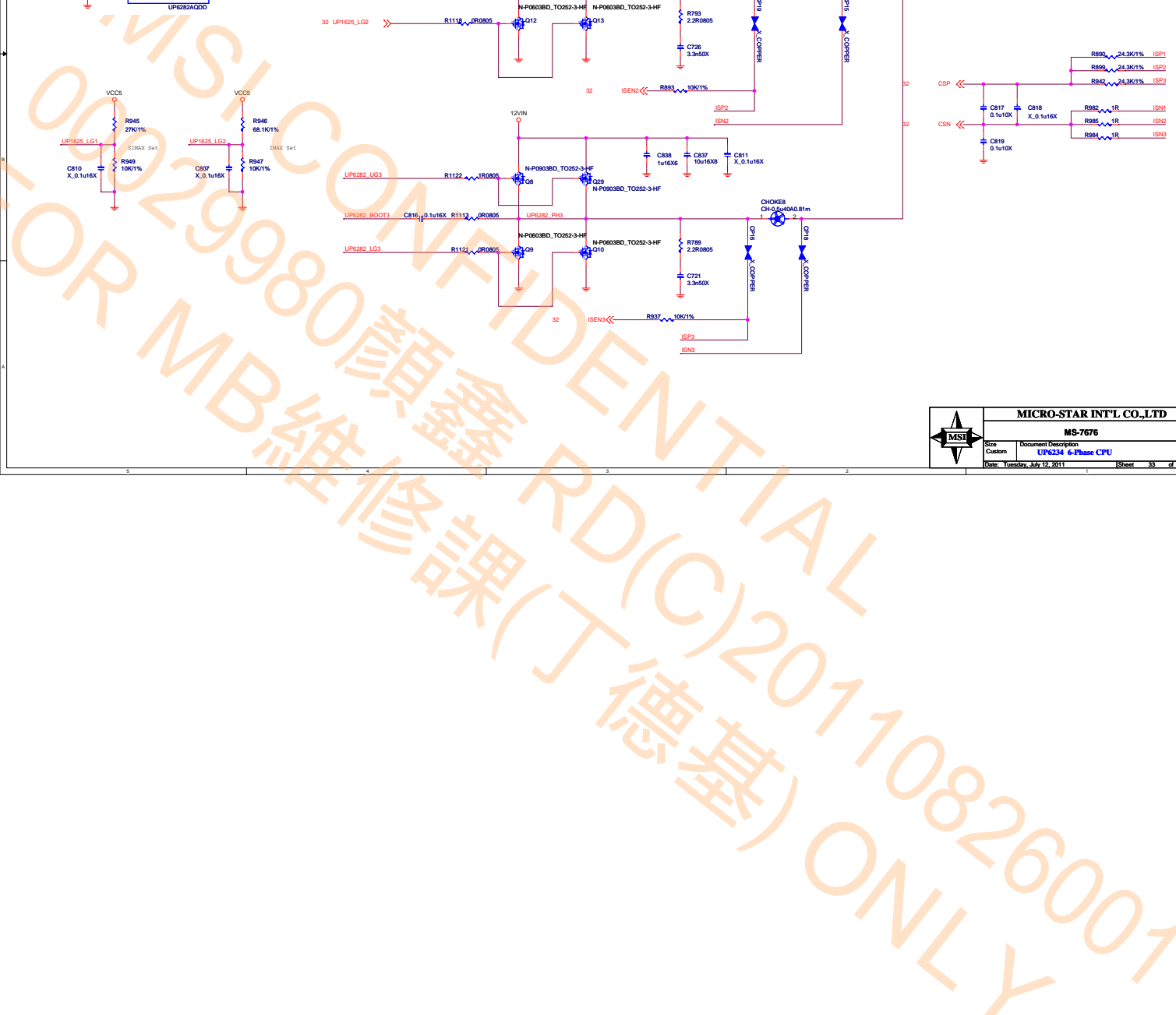
$I_{ripple} = 1.80A$
 $5.08 * 1 = 5.08A > 1.80A$

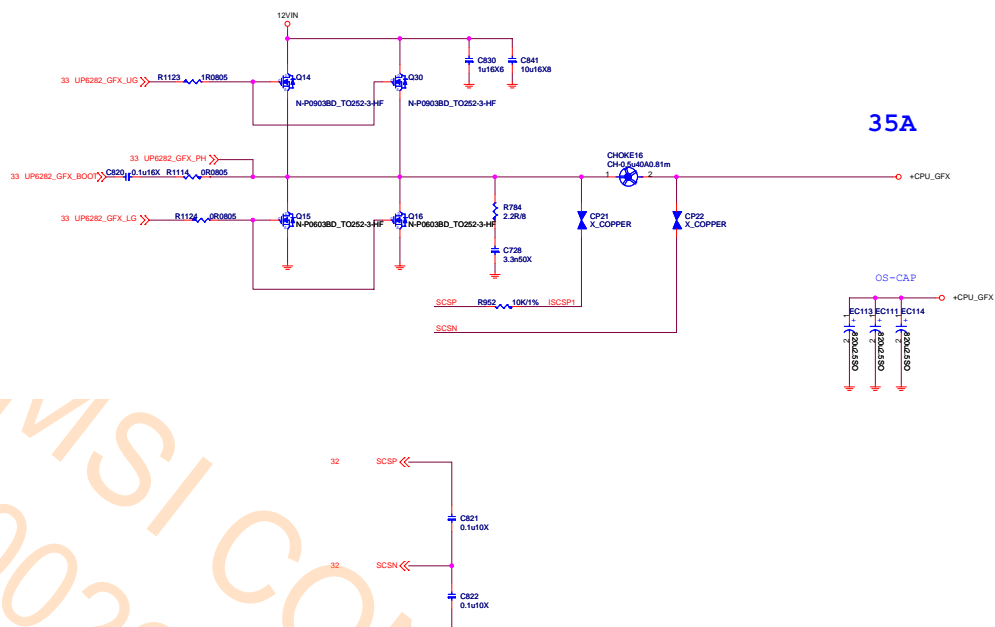


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Custom	PCH Power - uP6103 I-Phase		3.1
Part No.: MS-7676 Rev 3.1 Date: 9/1/98			

VRMPWRGD LEVEL SHIFT







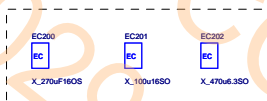
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Custom	UP6234 1-Phase GPU	3.1	
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MS-7680-4.0			
OPT	Configure	BOM	Function
	H61MU-S01 (B3)	601-7680-120	MS-7680 40 H61MU-S01 (B3), H61+2DDR3+1*PCI_Ex16+3*PCI_Ex1+4*SATAII+HD 8CH Audio+10USB2.0+2USB3.0+Gb LAN, (EuP), RoHS
A	H61MU-E34 (B3)	601-7680-11S	MS-7680 40 OPT:A H61M-E34 (B3) Intel H61+2*DDRIII+1*PCIe16, 2*PCIe1, 1*PCI+ DVI/D-sub/HDMI+4*SATAII+10*USB2+HD8CH Audio+Gb lan, EuP, (All Solid Cap), RoHS

AUDIO CON OPT.



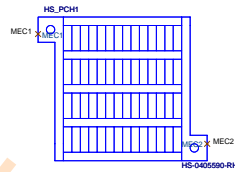
EL/OS OPT.



LABEL OPT.



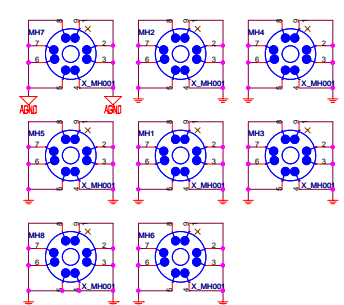
PCH XDP PWRGD/RESET



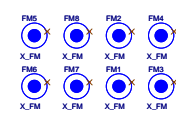
Simulation



Mounting Holes



Optical Fiducial Marks-120



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